MediaTek

MT6305B GSM Power Management System

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Revision: 1.0

Release Date: Feb, 25, 2005

Product Change Notice

Original product name : MT6305N/FT
New identification : MT6305BN/CY

Change Contents

Item	Change type	Description	Reason for change
1	New function	Use pin#3 (original NC pin) to program VCORE/VRTC. VCORE/VRTC=1.8V/1.5V as pin#3 is floating. VCORE/VRTC=1.2V/1.2V as pin#3 is GND.	Provide alternative VCORE/VRTC voltage.
2	Device protection	CHRIN can be up to 15V but the charger will be off automatically when CHRIN>Vac_limit. The spec. of Vac_limit is 8~9.5V. It can't be used with external linear charger.	To protect internal device.

Special request on PCB

- It must use X5R-type decoupling capacitor on VTCXO and VA LDO outputs for good performance against temperature variation.
- In VCORE/VRTC=1.8V/1.5V application, no special change is required to use MT6305BN/CY. It's fully compatible with the PCB for MT6305N/FT. If user would like to configure VCORE/VRTC=1.2V/1.2V, just tie pin#3 to GND via a 0-Ohm resistor.

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Revision History

Revision	Date	Author	Comments
1.0	Feb. 25, 2005	Cathy Chen	First Release of MT6305B Differences from the data sheet of MT6305 Rev.1.4 : 1. Add PCN on page 2 2. Update Abstract on page 5 3. Update charger input feature on page 8 4. Ordering information on page 8 5. Pin configuration on page 8 (pin#3, pin#29, pin#30) 6. Add VCORE=1.2V spec. (1.1V~1.3V) on page 9 7. Add VRTC=1.2V spec. (1.1V~1.3V) on page 10 8. Modify reference voltage to 1.170V~1.190V on page 10 9. Modify reset on delay time per unit cap. to 1~3ms/nF on page 11 10. Add Valid_CHRIN maximum CHRIN voltage spec. (8~9.5V) on page 9 11. Modify Chr_Det on/off threshold to 3.0% on page 11 12. Modify Gatedrv VOH and VOL on page 11 13. Update Electrical Characteristics Waveform from page 13 to page 21 14. Update pin description on page 22 according to the updated pin configuration 15. Update fig.1 and fig.3 according to the new pin configuration 16. Update the detailed descriptions of VCORE, VRTC and Charge detection 17. Modify the LDO capacitor selection note in the applications information section on page 29 18. Add one layout guideline note on page 29

Revision	Date	Reviewer	Comments
1.0	Feb. 25, 2005	Maxwell Hsu	First Release

Revision	Date	Leader	Comments

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Abstract

The MT6305BN/CY is a power management system chip optimized for GSM handsets, especially those based on the MediaTek MT62xx system solution. It contains seven LDOs, one to power each of the critical GSM sub-blocks. The integrated LDOs are designed for low power and low noise, such as Va and Vtcxo. Vcore, Vrtc, Vm and Vsim provide alternative output voltages for system design flexibility. Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm.

The MT6305 is optimized for maximum battery life, featuring a ground current of only 108µA and 187µA when the phone is in standby and operation respectively. For battery charging, the MT6305 can be used with lithium ion (Li+) and nickel metal hydride (NiMH) batteries. It contains three open-drain output switches for LED, alerter and vibrator control. The SIM interface provides the level shift between SIM card and microprocessor.

In addition, MT6305 provides other features including current limiting, under voltage lock-out protection, deep discharge lockout protection and over temperature protection.

MT6305BN/CY is offered in 48-pin QFN package. The tiny size and low profile reduce the required board area and increase the power density of the whole power system design.

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GSM Power Management System

Features

- **Handles all GSM Baseband Power Management**
- **2.8V to 5.5V Input Range**
- **Charger Input up to 15V, automatically terminate charging above 9V**
- **Seven LDOs Optimized for Specific GSM Subsystems**
- **High Operation Efficiency and Low Stand-by Current**
- **Li-Ion and NiMH Battery Charge function**
- **SIM Card Interface**
- **Three Open-Drain Output Switches to Control the LED, Alerter and Vibrator**
- **Thermal Overload Protection**
- **Under Voltage Lock-out Protection**
- **Over Voltage Protection**
- **Power-on Reset and Start-up Timer**
- **48-Pin QFN Package**

Applications

- **GSM/GPRS Mobile Handsets**
- **Basic Phone and High-end Phone**

General Description

The MT6305 is a power management system chip optimized for GSM handsets, especially those based on the MediaTek MT62xx system solution. It contains seven LDOs, one to power each of the critical GSM sub-blocks. Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm. The MT6305 is optimized for maximum battery life, featuring a ground current of only 108µA and 187µA when the phone is in standby and operation respectively.

The MT6305 battery charger can be used with lithium ion (Li+) and nickel metal hydride (NiMH) batteries.

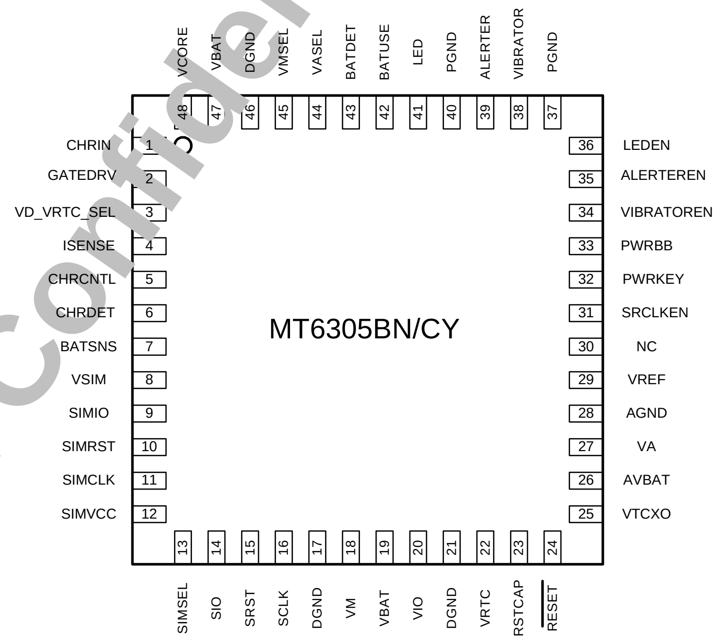
The MT6305 contains three open-drain output switches for LED, alerter and vibrator control. The SIM interface provides the level shift between SIM card and microprocessor.

The MT6305 is available in 48-pin QFN package. The operating temperature range is from -25°C to +85°C.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE
MT6305Q1X	MT6305BN/CY	-25°C to +85°C	QFN - 48L

Pin Configuration



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Absolute Maximum Ratings

CHRIN and GATEDRV relative to GND....-0.3V to 15V
LED, ALERTER, VIBRATOR and VREF relative to GND……………………………..…...…….-0.3V to Vbat+0.3V
All other pins relative to GND……………….-0.3V to 7V
Operating Temperature Ranges..…..…-25°C to +85°C
Maximum Junction Temperature ……..……….+165°C
Storage Temperature Range…..…..…-65°C to +165°C
Thermal Impedance, θ_{JA}(4 layer JEDEC PCB)....23°C/W
Reflow Temperature (soldering, 10sec)…........+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Vbat=3V-5.5V, CVa=4.7µF, CVrtc=0.22µF, CVcore=CVm=CVref=CVtcxo=CVsim=CVio=2.2µF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Main Controller					
Battery Input Voltage Range		3	---	5.5	V
Charger Input Voltage Range		---	---	15	V
Valid_CHRIN maximum CHRIN voltage	Charger will terminate charging automatically when CHRIN is above the voltage	8.0	9.0	9.5	V
Shutdown Supply Current	Vbat<2.5V 2.5V<Vbat<3.2V 3.2V<Vbat	---	20 45 45	40 75 80	µA
Operation Ground Current	All Output on Vtcxo off, all others on Va, Vtcxo off, all others on	---	187 148 108	500 200 150	µA
UVLO on Threshold	Vbat; Falling edge	2.85	2.9	2.95	V
UVLO Hysteresis	Vbat	250	300	350	mV
Deep Discharging Lockout on Threshold	Vbat Falling edge	2.35	2.5	2.65	V
Deep Discharging Lockout Hysteresis	Vbat	100	200	300	mV
Thermal Shutdown Threshold		---	165	---	°C
Thermal Shutdown Hysteresis		---	40	---	°C
LDO Enable Response Time		---	250	---	µs
Power Key Input High Voltage	PWRKEY	0.7xVbat	---	---	V
Power Key Input Low Voltage	PWRKEY	---	---	0.3xVbat	V
PWRBB Input High Voltage	PWRBB	1	---	---	
PWRBB Input Low Voltage	PWRBB	---	---	0.2	
Control Input High Voltage	VMSEL, SIMSEL, SIMVCC, SRCLKEN, VASEL, BATUSE, LEDEN, VIBRATOREN, ALERTEREN	2	---	---	V
Control Input Low Voltage		---	---	0.8	V
Digital Core Voltage LDO (Vcore)					
1.8V Output Voltage		1.7	1.8	1.9	V
1.2V Output Voltage		1.1	1.2	1.3	V
Output Short Current Limit		---	430	---	mA
Load Regulation	0.05mA <I_load< 200mA	---	1.3	20	mV
Line Regulation	3.6V <Vbat< 5.5V	---	3.3	6	mV
Digital IO Voltage LDO (Vio)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit		---	275	---	mA
Load Regulation	0.05mA<I_load<100mA at Vbat=3.6V	---	3	10	mV

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Electrical Characteristics (continued)

(Vbat=3V-5.5V, CVa=4.7μF, CVrtc=0.22μF, CVcore=CVm=CVref=CVtcxo=CVsim=CVio=2.2μF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Line Regulation	3.6V<Vbat<5.5V	---	4.6	7	mV
Analog Voltage LDO (Va)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit		---	400	---	mA
Load Regulation	0.05mA<I_load<150mA at Vbat=3.6V	---	3.3	10	mV
Line Regulation	3.6V<Vbat<5.5V	---	0.4	7	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz	---	50	---	μVrms
Ripple Rejection	Frequency from 10Hz to 3kHz Frequency from 3kHz to 1MHz	---	65 40	---	dB
VTCXO Voltage LDO (Vtcxo)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit		---	45	---	mA
Load Regulation	0.05mA<I_load<20mA at Vbat=3.6V	---	0.1	5	mV
Line Regulation	3.6V<Vbat<5.5V	---	0.4	3.5	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz	---	50	---	μVrms
Ripple Rejection	Frequency from 10Hz to 3kHz Frequency from 3kHz to 1MHz	---	65 40	---	dB
RTC Voltage LDO (Vrtc)					
1.5V Output Voltage		1.3	1.5	1.65	V
1.2V Output Voltage		1.1	1.2	1.3	V
Output Short Current Limit		---	1.35	---	mA
Off Reverse Input Current		---	0.02	1	μA
Memory Voltage LDO (Vm)					
1.8V Output Voltage		1.7	1.8	1.9	V
2.8V Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit		---	315	---	mA
Load Regulation(1.8V) Load Regulation(2.8V)	0.05mA<I_load<150mA at Vbat=3.6V	---	2.7 4.4	10 10	mV
Line Regulation(1.8V) Line Regulation(2.8V)	3.6V<Vbat<5.5V	---	2.6 2.8	5 7	mV
SIM Voltage LDO (Vsim)					
1.8V Output Voltage		1.65	1.8	1.95	V
3.0V Output Voltage		2.82	3.0	3.18	V
Output Short Current Limit		---	38	---	mA
Load Regulation(1.8V) Load Regulation(3.0V)	0.05mA<I_load<20mA at Vbat=3.6V	---	1 1.7	10 10	mV
Line Regulation(1.8V) Line Regulation(3.0V)	3.6V<Vbat<5.5V	---	1.2	5 8	mV
Reference Voltage Output					
Reference Voltage		1.170	1.180	1.190	V
Line Regulation	3.0V<Vbat<5.5V without load	---	0.3	2	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz	---	40	---	μVrms
Ripple Rejection	Frequency at 217Hz	65	75	---	dB
Reset Generator-					

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Electrical Characteristics (continued)

(Vbat=3V-5.5V, CVa=4.7µF, CVrtc=0.22µF, CVcore=CVm=CVref=CVtcxo=CVsim=CVio=2.2µF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reset Output High Voltage		Vio-0.5	---	---	V
Reset Output Low Voltage		---	---	0.2	V
Reset Output Current		---	1	---	mA
Reset on Delay Time per unit Cap.		1	2	3	ms/nF
LED/Alerter/Vibrator Driver					
Sink Current of LED Driver	Von<0.5V	150	---	---	mA
Sink Current of Alerter Driver	Von<0.5V	300	---	---	mA
Sink Current of Vibrator Driver	Von<0.5V	250	---	---	mA
Battery Charger					
Charge Output Voltage (Li-ion Battery)	BATUSE=0	4.15	4.2	4.25	V
Charge Output Voltage (NiMH Battery)	BATUSE=1	5	5.1	5.2	V
Chr_Det On Threshold	(Chrin-Vbat)/Vbat, Chrin>4V	---	3.0	---	%
Chr_Det Off Threshold	(Chrin-Vbat)/Vbat, Chrin>4V	---	3.0	---	%
Pre-charge Current	Vbat<1.5V	5	---	15	mA
Pre-charging Current Threshold Voltage	Vbat>2V;UVLO Active, R1=0.2Ω	5	10	15	mV
Constant Charge Current Threshold Voltage	Vbat>3.2V; R1=0.2Ω	135	160	185	mV
Gatedrv output high voltage	I=-0.1mA	Vchrin-1.0V	---	---	V
Gatedrv output low voltage	I=0.1mA	---	---	0.9	V
GSM Interface					
Vih(SIMCLK,SIMRST)		Vio-0.6	---	---	V
Vil (SIMCLK,SIMRST)		---	---	0.6	V
Vilsimio	Vol≦0.4V, Iol=1mA	---	---	0.23	V
	Vol≦0.4V, Iol=0mA	---	---	0.335	V
Vihsimio , Vohsimio	Iih,Ioh=± 20µA	Vio-0.6	---	---	V
Iilsimio	Vil=0V	---	---	-0.9	mA
Volsimio	Vil=0.4V	---	---	0.42	V
SIMIO Pull-up Resistance to Vio		16	20	24	KΩ
Interface to 3V SIM card					
Volrst	I=20µA	---	---	0.4	V
Vohrst	I=-200µA	0.9Vsim	---	---	V
Volclk	I=20µA	---	---	0.4	V
Vohclk	I=-200µA	0.9Vsim	---	---	V
Vil		---	---	0.4	V
Vihsio , Vohsio	I=± 20µA	Vsim-0.4	---	---	V
Iil	Vil=0V	---	---	-1	mA
Vol	Iol=1mA , SIMIO≦0.23V	---	---	0.4	V
Interface to 1.8V SIM card					
Volrst	I=20µA	---	---	0.2Vsim	V
Vohrst	I=-200µA	0.9Vsim	---	---	V
Volclk	I=20µA	---	---	0.2Vsim	V
Vohclk	I=-200µA	0.9Vsim	---	---	V
Vil		---	---	0.4	V
Vihsio , Vohsio	I=± 20µA	Vsim-0.4	---	---	V
Iil	Vil=0V	---	---	-1	mA

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Electrical Characteristics (continued)

(Vbat=3V-5.5V, CVa=4.7µF, CVrtc=0.22µF, CVcore=CVm=CVref=CVtcxo=CVsim=CVio=2.2µF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Vol	Iol=1mA , SIMIO≦0.23V	---	---	0.4	V
SIM Card Interface Timing					
SIO Pull-up Resistance to Vsim		8	10	12	KΩ
SRST, SIO rise/fall time	Vsim=3/1.8V, load with 30pF	---	---	1	µS
SCLK rise/fall time	Vsim=3V, CLK load with 30pF	---	---	18	nS
	Vsim=1.8V, CLK load with 30pF	---	---	50	nS
SCLK frequency	CLK load with 30pF	5	---	---	Mhz
SCLK duty cycle	SIMCLK Duty=50%, fsimclk=5Mhz	47	---	53	%
SCLK Propogation Delay		---	30	50	nS

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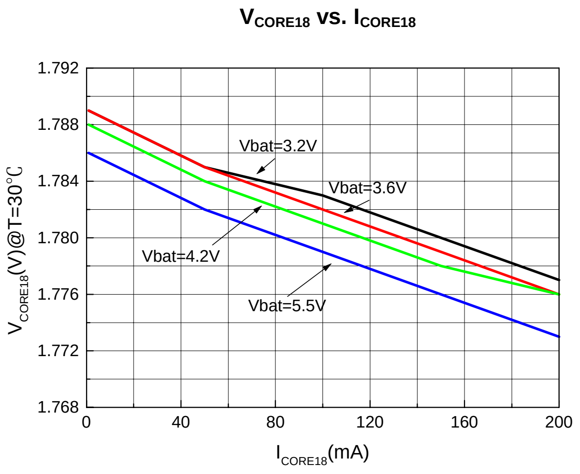
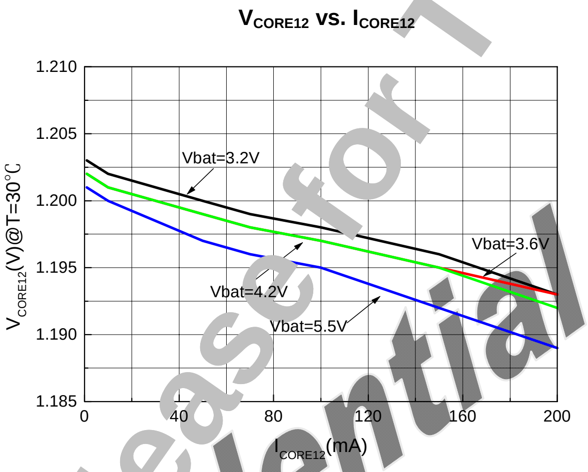
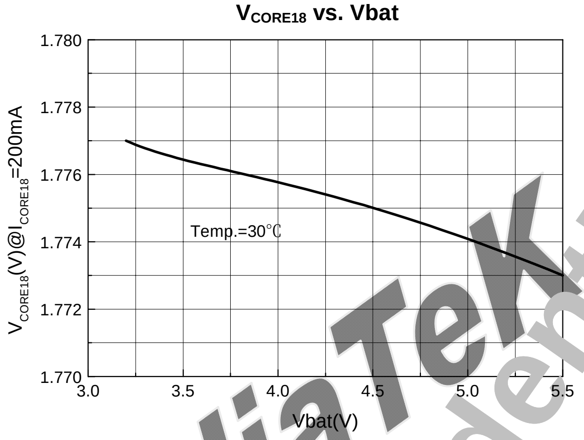
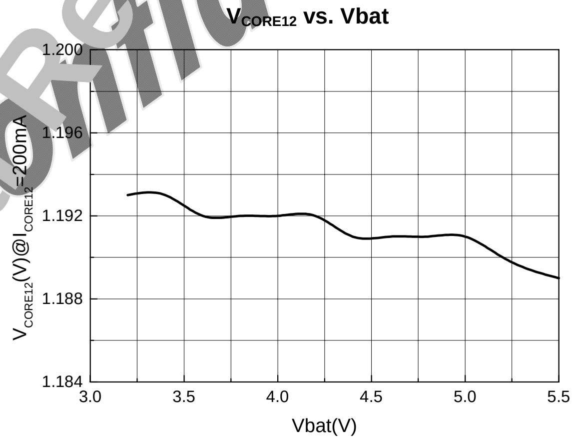
Electrical Characteristics Waveform

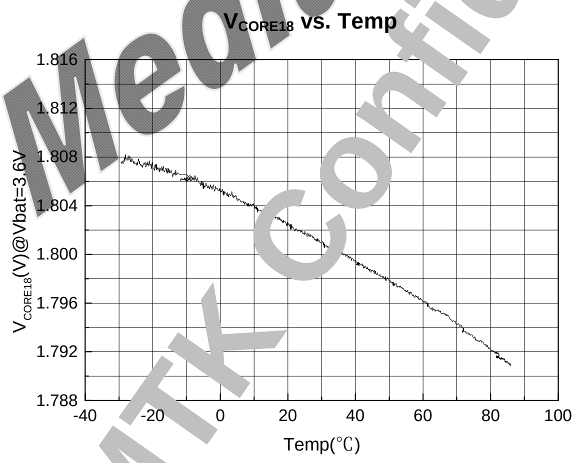
(Vbat=3V-5.5V, CVa=4.7μF, CVrtc=0.22μF, CVcore=CVm=CVref=CVtcxo=CVsim=CVio=2.2μF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

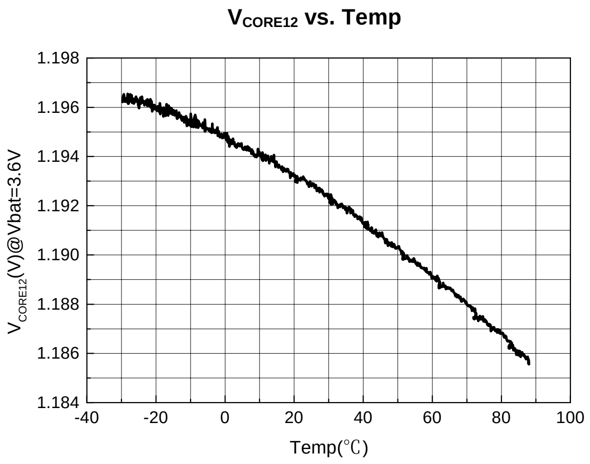












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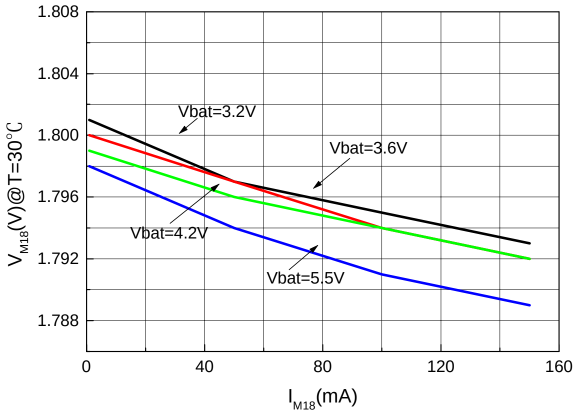
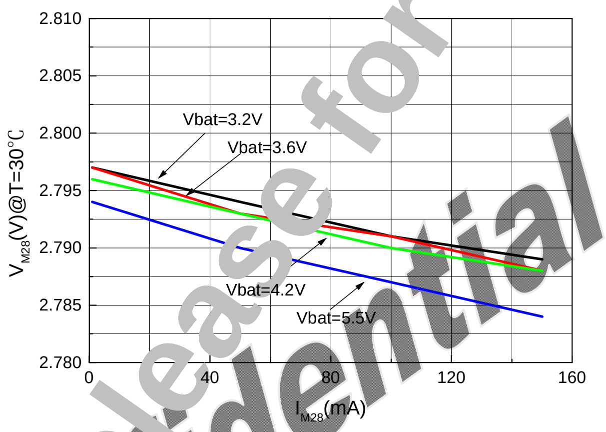
Electrical Characteristics (continued)

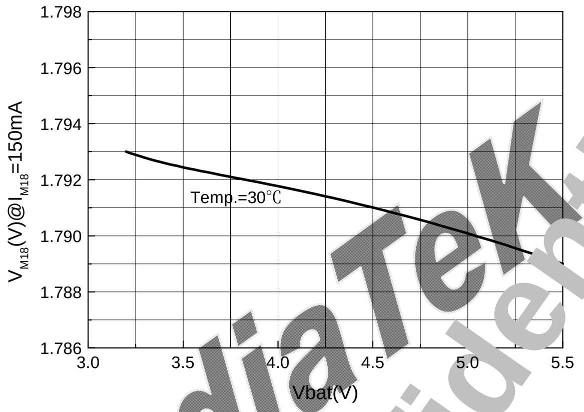
V_{M18} vs. I_{M18}



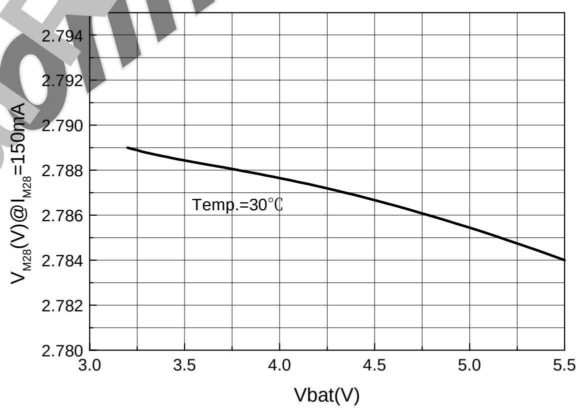
V_{M28} vs. I_{M28}



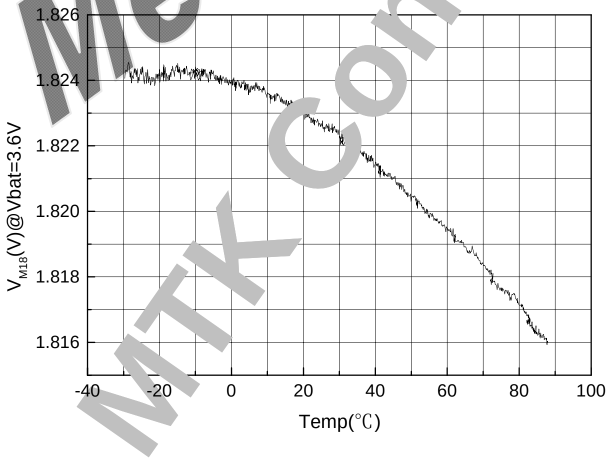
V_{M18} vs. Vbat



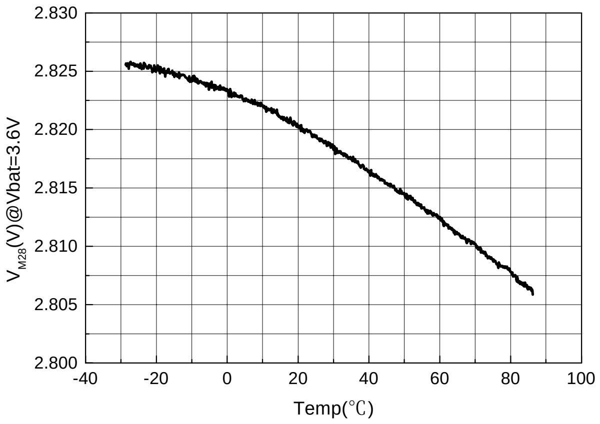
V_{M28} vs. Vbat



V_{M18} vs. Temp



V_{M28} vs. Temp



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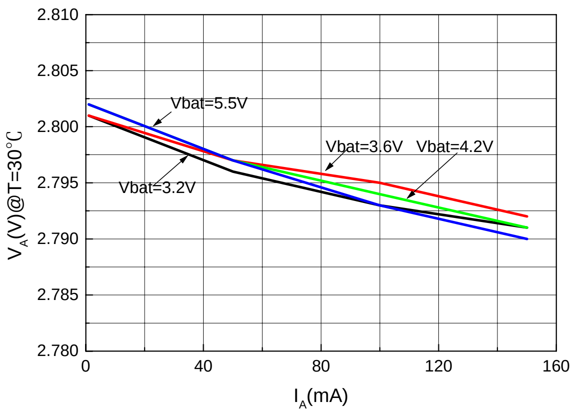
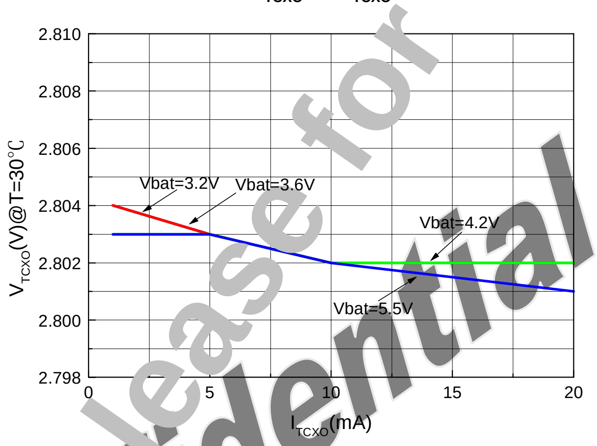
Electrical Characteristics (continued)

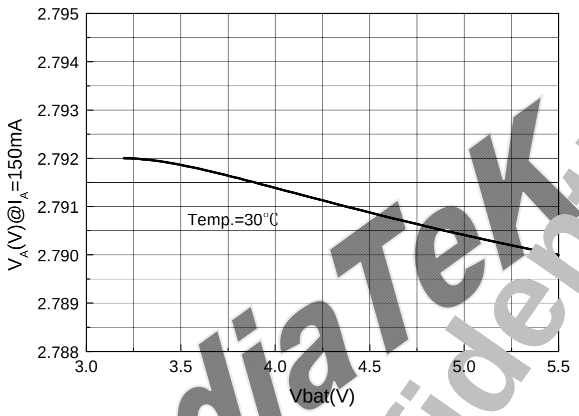
V_A vs. I_A



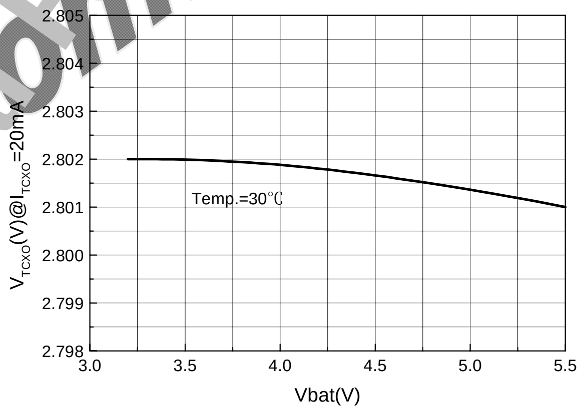
V_{TCXO} vs. I_{TCXO}



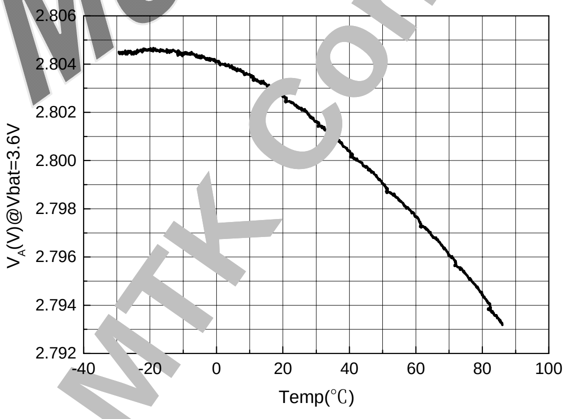
V_A vs. Vbat



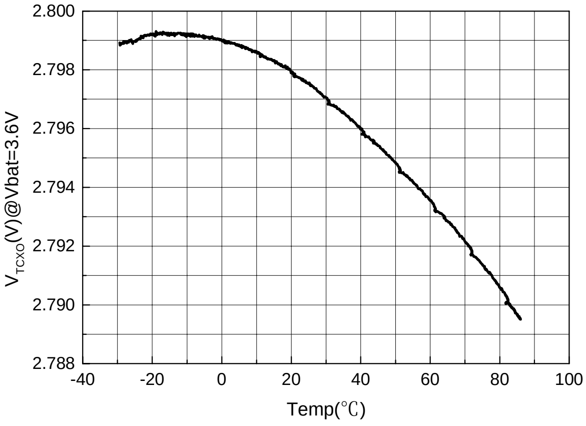
V_{TCXO} vs. Vbat



V_A vs. Temp



V_{TCXO} vs. Temp



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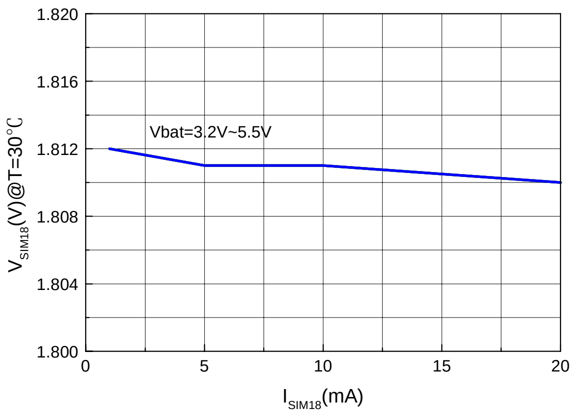
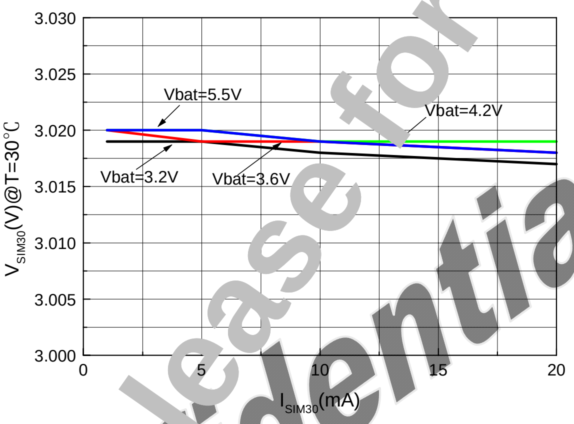
Electrical Characteristics (continued)

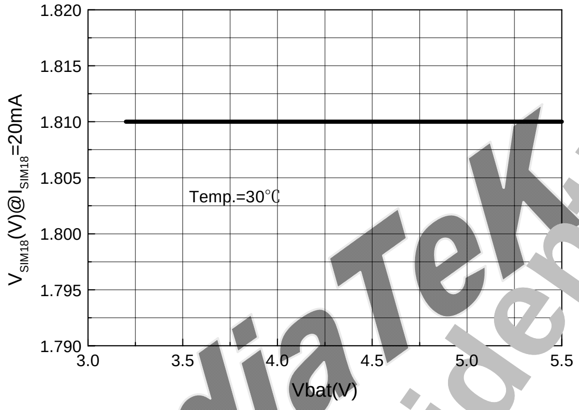
V_{SIM18} vs. I_{SIM18}



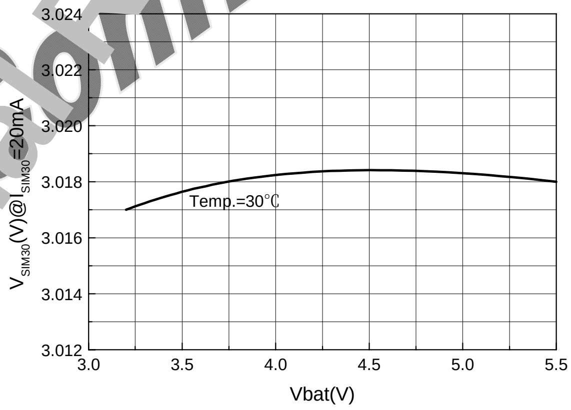
V_{SIM30} vs. I_{SIM30}



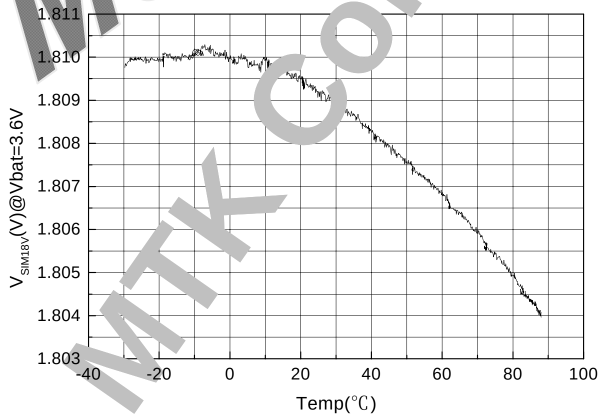
V_{SIM18} vs. Vbat



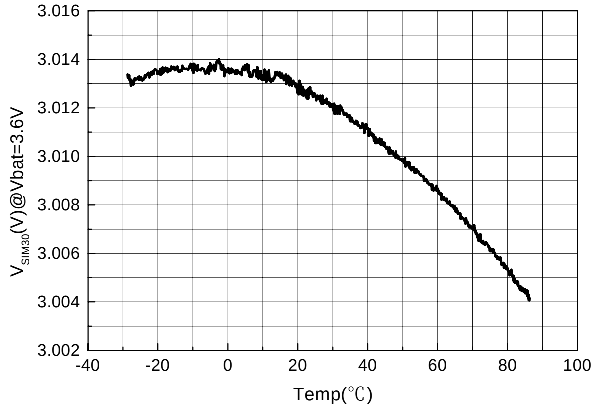
V_{SIM30} vs. Vbat



V_{SIM18} vs. Temp



V_{SIM30} vs. Temp



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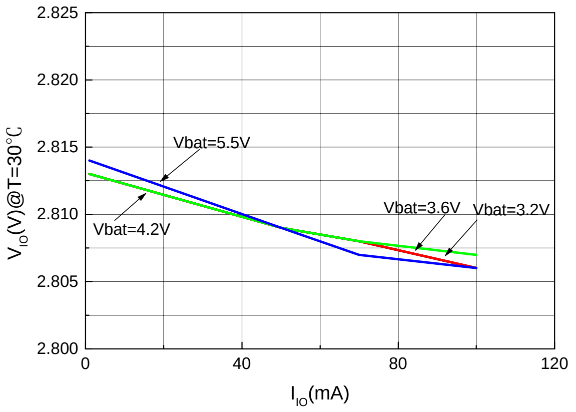
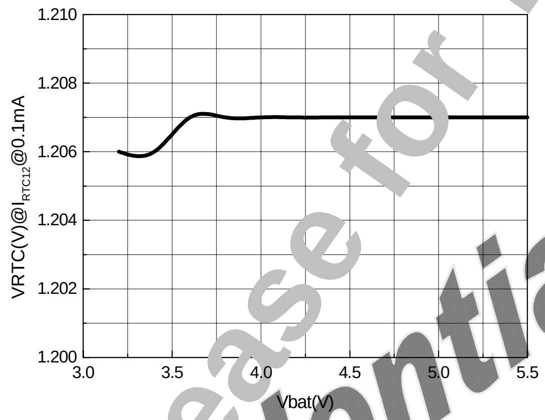
Electrical Characteristics (continued)

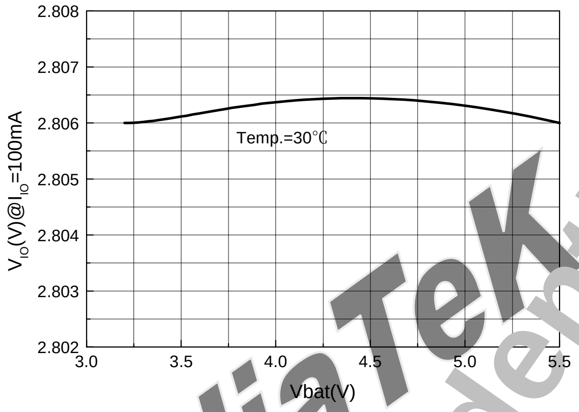
V_{IO} vs. I_{IO}



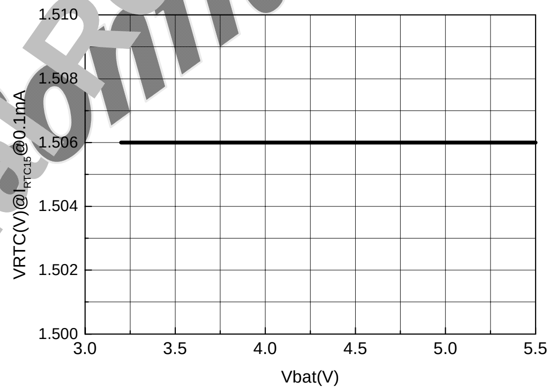
V_{RTC12} vs. Vbat



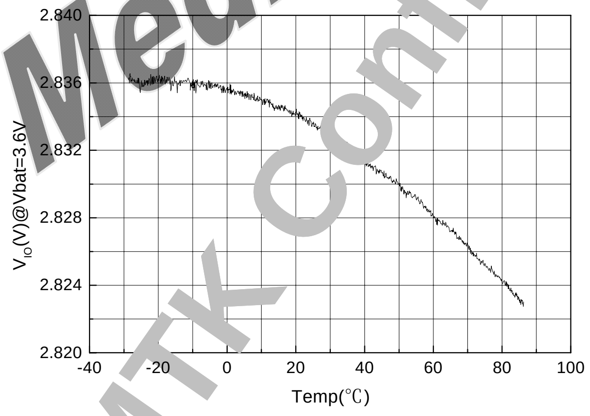
V_{IO} vs. Vbat



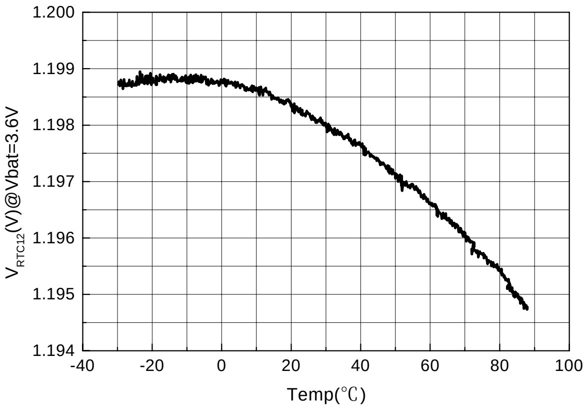
V_{RTC15} vs. Vbat



V_{IO} vs. Temp



V_{RTC12} vs. Temp



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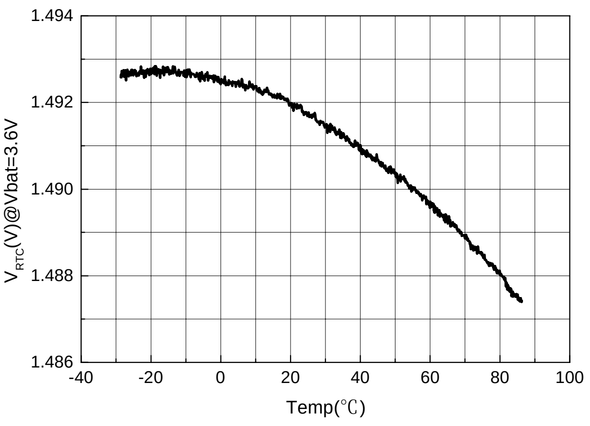
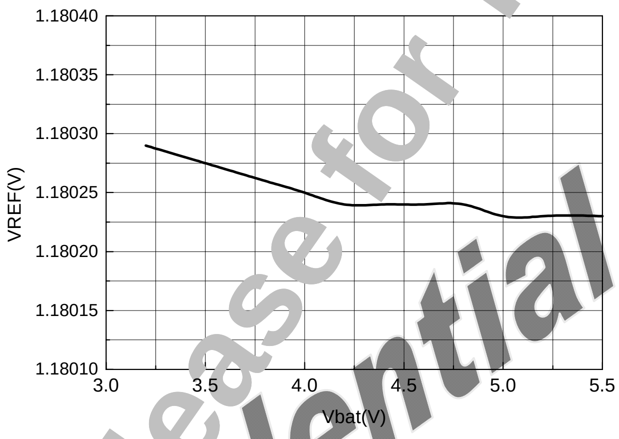
Electrical Characteristics (continued)

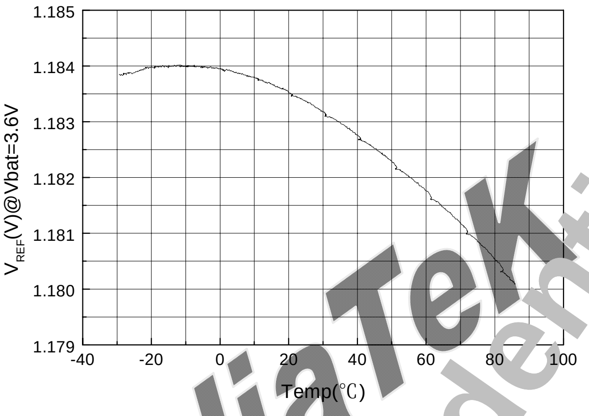
V_{RTC15} vs. Temp



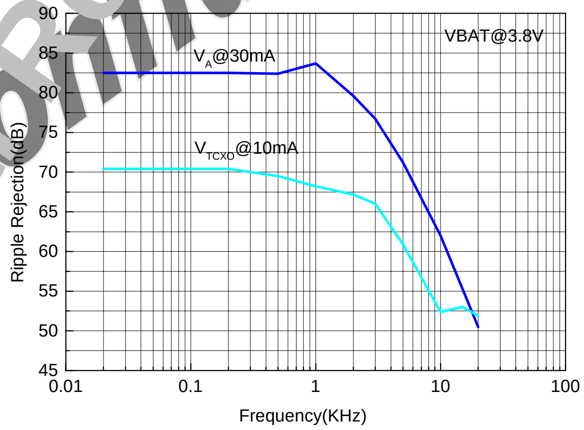
V_{REF} vs. Vbat



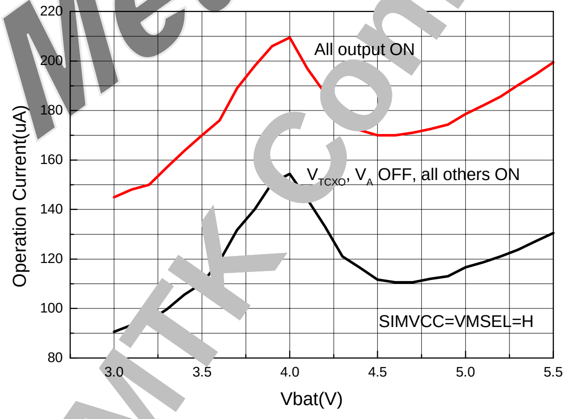
V_{REF} vs. Temp



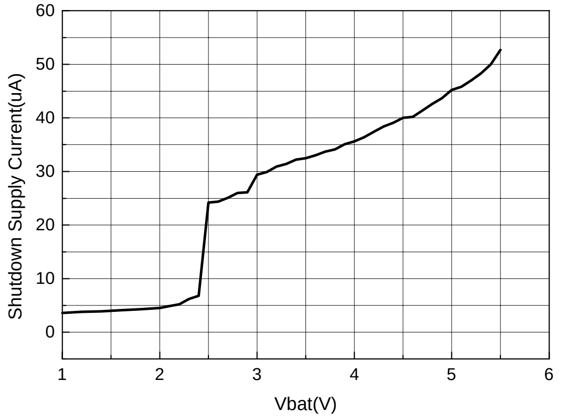
V_A & V_{TCXO} Ripple Rejection vs. Frequency



Operation Current vs. Vbat



Shutdown Current vs. Vbat



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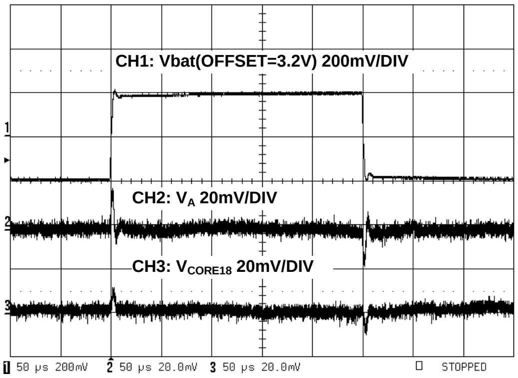
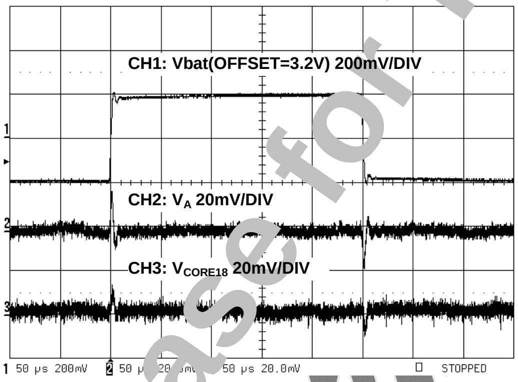
Electrical Characteristics (continued)

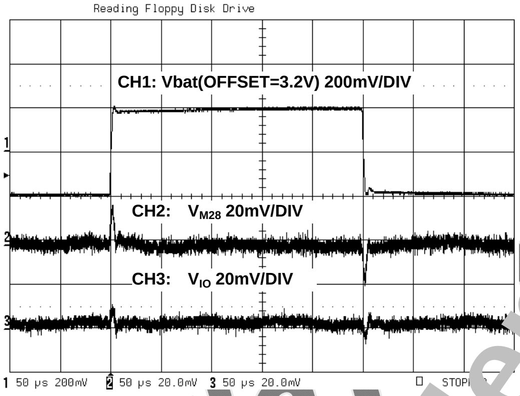
Line Transient, Min. Load



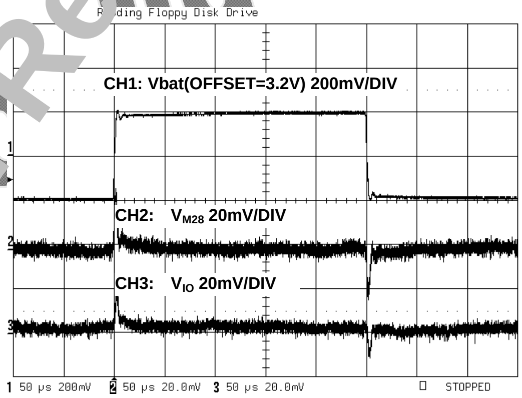
Line Transient, Max. Load



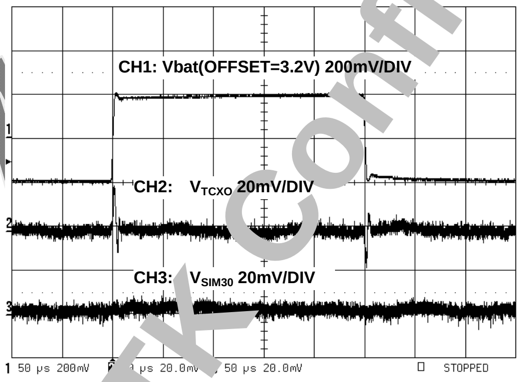
Line Transient, Min Load



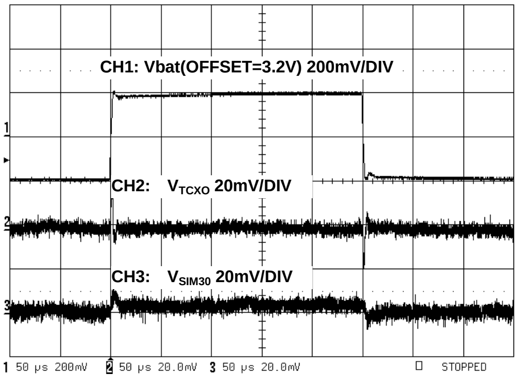
Line Transient, Max. Load



Line Transient, Min Load



Line Transient, Max. Load



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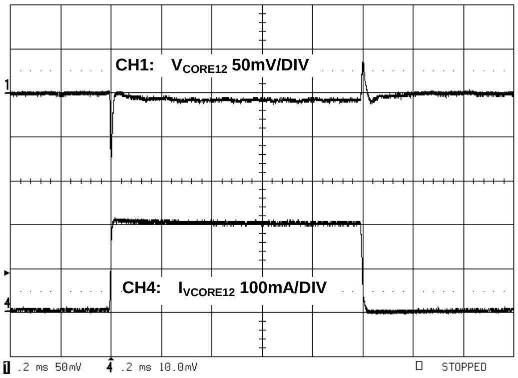
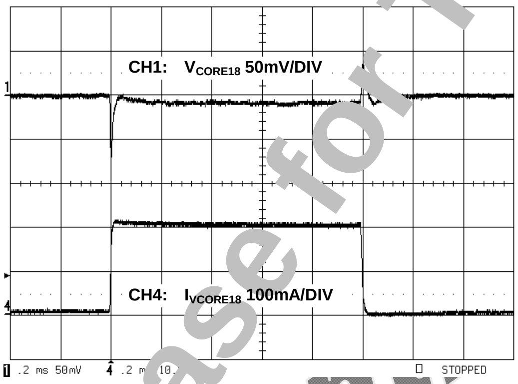
Electrical Characteristics (continued)

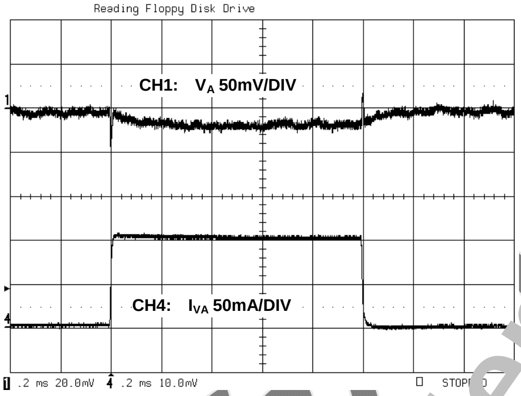
V_{CORE12} Load Transient



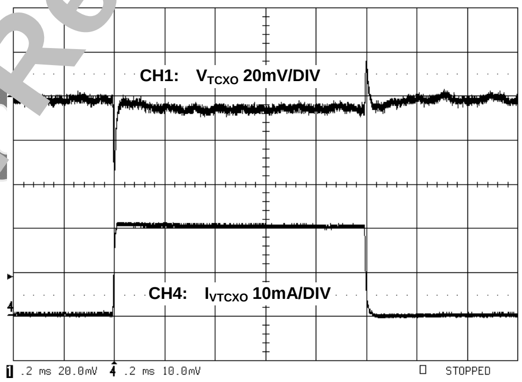
V_{CORE18} Load Transient



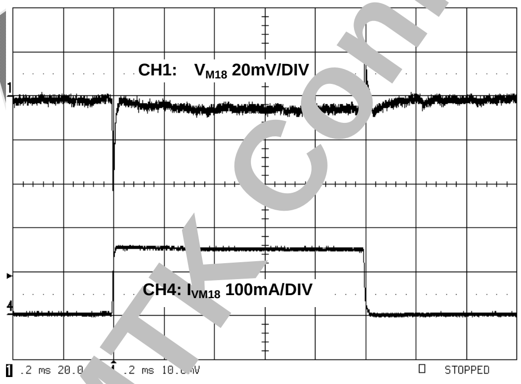
V_A Load Transient



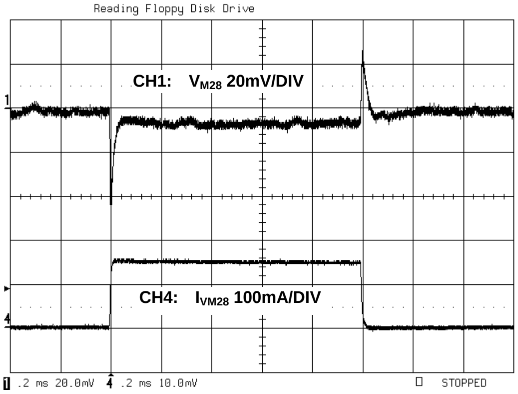
V_{TCXO} Load Transient



V_{M18} Load Transient



V_{M18} Load Transient



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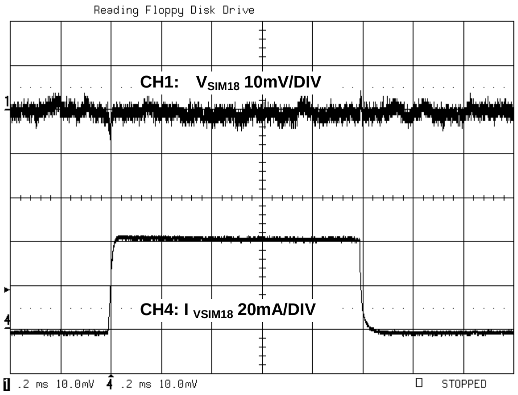
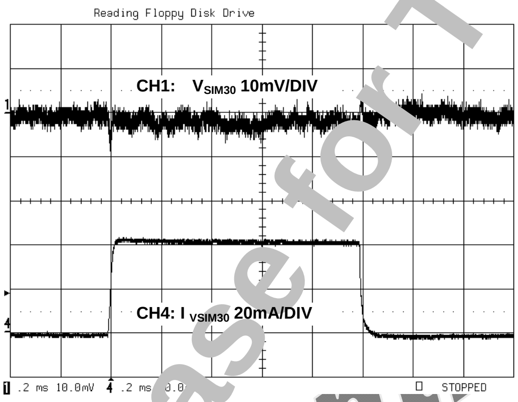
Electrical Characteristics (continued)

V_{SIM18} Load Transient



V_{SIM30} Load Transient



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Pin Description

PIN	NAME	FUNCTION
1	CHRIN	Charger Input Voltage
2	GATEDRV	Gate Drive Output
3	VD_VRTC_SEL	Floating or High for VCORE/VRTC=1.8V/1.5V, Low for VCORE/VRTC=1.2V/1.2V
4	ISENSE	Charger Current Sense Input
5	CHRCNTL	Microprocessor Control Input Signal for Gate Drive, Internal Pull Low to DGND
6	CHRDET	Charger Detect Output
7	BATSNS	Battery Input Voltage Sense
8	VSIM	SIM Supply
9	SIMIO	Non-Level-Shifted Bidirectional Data I/O
10	SIMRST	Non-Level-Shifted SIM Reset Input, Internal Pull High to VIO
11	SIMCLK	Non-Level-Shifted SIM Clock Input
12	SIMVCC	SIM Enable
13	SIMSEL	High for Vsim=3.0V, Low for Vsim=1.8V
14	SIO	Level-Shifted SIM Bidirectional Data Input/Output
15	SRST	Level-Shifted SIM Reset Output
16	SCLK	Level-Shifted SIM Clock Output
17,21,46	DGND	Digital Ground
18	VM	Memory Supply
19	VBAT	Battery Input Voltage
20	VIO	Digital IO Supply
22	VRTC	Real Time Clock Supply
23	RSTCAP	Reset Delay Time Capacitance
24	/RESET	System Reset, Low Active
25	VTCXO	TCXO Supply
26	AVBAT	Battery Input Voltage for Analog Block Circuits
27	VA	Analog Supply
28	AGND	Analog Ground
29	VREF	Reference Voltage Output
30	NC	
31	SRCLKEN	VTCXO and VA Enable
32	PWRKEY	Power on/off Key, Internal Pull High to VBAT
33	PWRBB	Power on/off Signal from Microprocessor
34	VIBRATOREN	Vibrator Driver Enable, Internal Pull Low to DGND
35	ALERTEREN	Alerter Driver Enable, Internal Pull Low to DGND
36	LEDEN	LED Driver Enable, Internal Pull Low to DGND
37,40	PGND	Power Ground
38	VIBRATOR	Vibrator Driver Input
39	ALERTER	Alerter Driver Input
41	LED	LED Driver Input
42	BATUSE	Battery Type Selection, High for NiMH, Low for Li-ion, Internal Pull Low to DGND
43	BATDET	Battery Detect Input, Low for Battery Connected, Internal Pull High for Battery Disconnected
44	VASEL	High for VA enabled with VTCXO, Low for VA enabled with VCORE, Internal Pull Low to DGND
45	VMSEL	High for Vm=2.8 V, Low for Vm=1.8V, Internal Pull High to VIO
47	VBAT	Battery Input Voltage
48	VCORE	Digital Core Supply

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Detailed Description Overview

The MT6305 is a power management chip optimized for use with GSM baseband chipsets in handset applications. Figure 1 shows the block diagram of the MT6305.

The MT6305 contains several blocks:

- **Seven Low Dropout Regulators (Core, Digital IO, Analog, Crystal Oscillator, Real-Time Clock, Memory, SIM)**
- **SIM Card Interface**
- **Vibrator, Alerter, and LED Drivers**
- **Power Sequence and Protection Logic**
- **Reset Generator**
- **Undervoltage Lockout**
- **Deep Discharge Lockout**
- **Battery Charger**

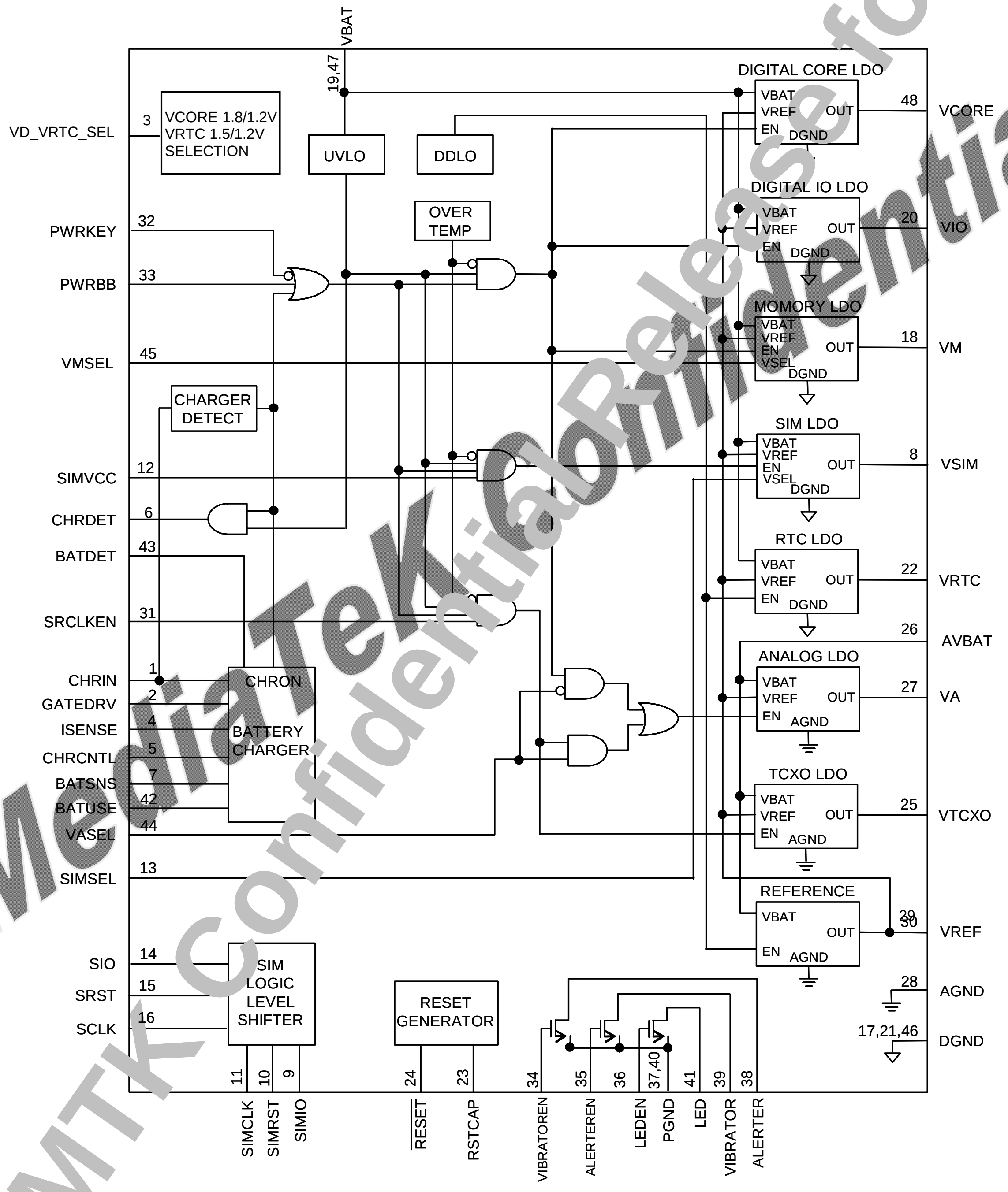

Figure 1. Functional Block Diagram

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Low Dropout Regulator (LDOs) and Reference

The MT6305 Integrates seven LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

Digital Core LDO (Vcore)

The digital core LDO is a regulator that could source 200mA (max) with 1.8V or 1.2V output voltage selection based on the supply voltage requirement of the baseband chipset. It supplies the baseband circuitry in the handset. The LDO is optimized for very low quiescent current.

Digital IO LDO (Vio)

The digital IO LDO is a regulator that could source 100mA (max) with 2.8V output voltage. It supplies the baseband circuitry in the handset. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

Analog LDO (Va)

The analog LDO is a regulator that could source 150mA (max) with 2.8V output voltage. It supplies the analog sections of the baseband chipsets. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the RF power amplifier burst frequency at 217Hz.

TCXO LDO (Vtcxo)

The TCXO LDO is a regulator that could source 20mA (max) with 2.8V output voltage. It supplies the temperature compensated crystal oscillator, which needs its own ultra low noise supply and very good ripple rejection ratio.

RTC LDO (Vrtc)

The RTC LDO is a regulator that could source 200µA (max) with 1.5V or 1.2V output voltage selection based on the system requirement. It charges up a capacitor-type backup coin cell to run the real-time clock module. The LDO features the reverse current protection and is optimized for ultra low quiescent current since it is always on except that battery voltage is below 2.5V.

Memory LDO (Vm)

The memory LDO is a regulator that could source 150mA (max) with 1.8V or 2.8V output voltage selection based on the supply specs of memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

SIM LDO (Vsim)

The SIM LDO is a regulator that could source 20mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules (SIM) card. It supplies the SIMs in the handset. The LDO is controlled independently of the others LDO.

Reference Voltage Output (Vref)

The reference voltage output is a low noise, high PSRR and high precision reference with a guaranteed accuracy of 1.5% over temperature. It is used as system reference in MT6305 internally. However for accurate specs of every LDO output voltage, avoid loading the reference voltage and bypass it to GND with 100 nF minimum.

SIM Card Interface

The SIM card interface circuitry of MT6305 meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband chipset to the SIM supply (Vsim). The bi-directional data bus is internal pull high with 20kohm resistor on the controller side and with 10kohm resistor on the SIM side.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV of human body mode ESD. In order to ensure proper ESD protection, careful board layout is required.

Vibrator, Alerter, LED Switches

Three built-in open-drain output switches drive the vibrator motor, alerter beeper and LEDs in the handset. Each switch is controlled by baseband chipset with enable pins. The switch of LED can sink 150mA to drive up to 10 LEDs simultaneously for backlight. The switch of vibrator can sink 250mA for a vibrator motor. The switch of alerter can sink 300mA to drive the beeper. And all the open-drain output switches are high impedance when disable.

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Power Sequence and Protection Logic

The MT6305 handles the powering ON and OFF of the handset. It is possible to start the power on sequence in three different ways:

- Pulling PWRKEY low
- Pulling PWRBB high
- CHRIN exceeds Chr_Det threshold

Pulling PWRKEY low is the normal way of turning on the handset. This will turn on Vcore, Vio, Vm LDOs as long as the PWRKEY is held low. The Vtcxo and Va LDOs is turned on when SRCLKEN is high. The microprocessor then starts and pulls PWRBB high after which PWRKEY can be released. Pulling PWRBB high will also turn on the handset. This is the case when the alarm in the RTC expires.

Applying an external supply on CHRIN will also turn the handset on. If MT6305 is in the UVLO state, applying the adapter will not start up the LDOs.

Table 1 shows states of the handset and the LDOs

Table 1. States of Mobile Handset and LDO

Phone State	CHRON	-UVLO	PWRBB (–PWRKEY)	SRCLKEN	Vrtc	Vd,Vio,Vm	Va, Vtcxo
No Battery or Vbat < 2.5V	X	L	X	X	Off	Off	Off
2.5V < Vbat < 3.2V	L	L	X	X	On	Off	Off
Pre-Charging	H	L	X	X	On	Off	Off
Charger-on	H	H	X	X	On	On	On
Switched off	L	H	L	X	On	Off	Off
Stand-by	L	H	H	L	On	On	Off
Active	L	H	H	H	On	On	On

Undervoltage Lockout (UVLO)

The UVLO function in the MT6305 prevents startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator trips and the threshold is reduced to 2.9V. This allows the handset to start normally until the battery decays to below 2.9V.

Once the MT6305 enters UVLO state, it draws very low quiescent current, typically 45µA. The RTC LDO is still running until the DDLO disables it. In this mode the MT6305 draws 20µA of quiescent current.

Deep Discharge Lockout (DDLO)

The DDLO in the MT6305 has two functions:

- To turn off the Vrtc LDO.
- To shut down the handset when the software fails to turn off the phone when the battery drops below 3.0V. The DDLO will shut down the handset when the battery falls below 2.5 V to prevent further discharge and damage to the cells.

Reset

The MT6305 contains a reset circuit that is active at both power-up and power-down. The RESET pin is held low at initial power-up, and the reset delay timer is started. The delay is set by an external capacitor on RSTCAP:

$$t_{RESET} = 2\frac{ms}{nF} \times C_{RSTCAP} \quad (1)$$

At power-off, RESET will be kept low.

Overtemperature Protection

If the die temperature of MT6305 exceeds 165°C, the MT6305 will disable all the LDOs except the RTC LDO. Once the overtemperature state is resolved, a new power on sequence is required to enable the LDOs.

Battery Charger

The MT6305 battery charger can be used with Li-ion and NiMH batteries. BATUSE pin can set MT6305 to fit the battery type. When BATUSE is set low, Li-ion battery is used. When BATUSE is set high, then NiMH battery is used. MT6305 charges the battery in three phases: pre-charging, constant current mode charging, and constant voltage mode charging. Figure 2 shows the flow chart of charger behavior. The circuitry of MT6305 combines with a PMOS transistor, diode, current-sense resistor externally to form a simple and low cost linear charger shown in Figure 3. MT6305 is available pulsed top-off charging algorithm by the CHRCNTL pin control from baseband chipset.

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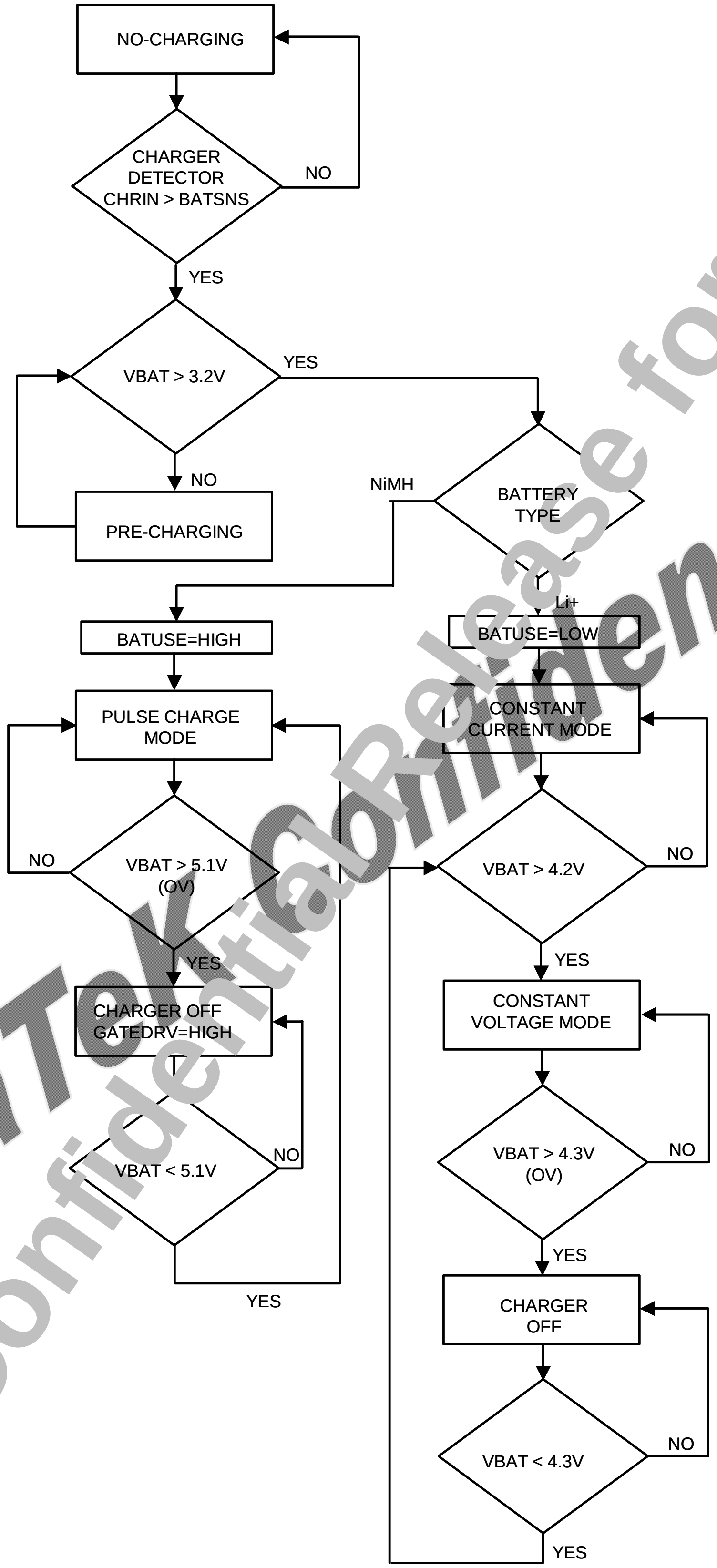

Figure 2. Battery Charger Flow Chart

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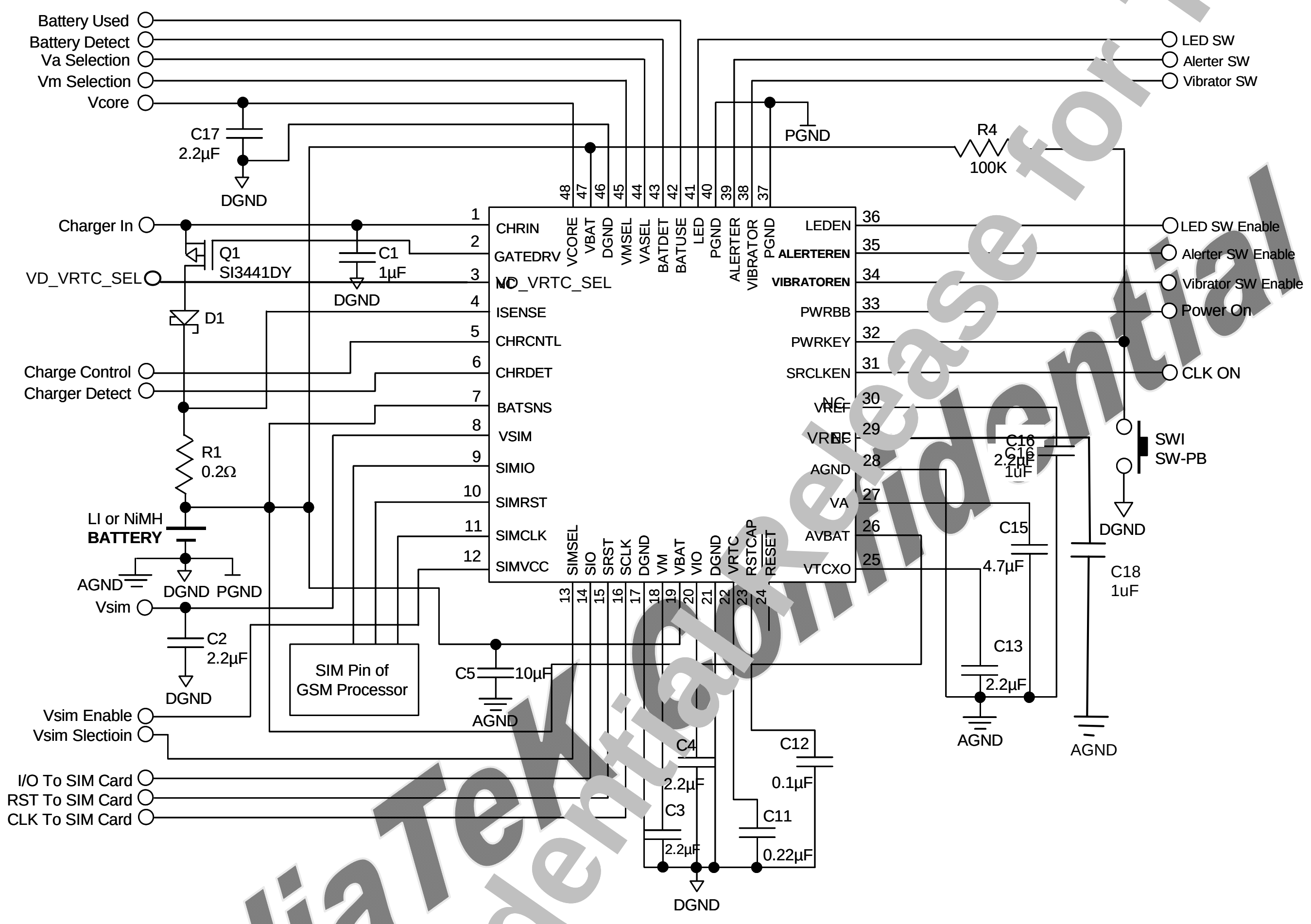

Figure 3. Typical Application Circuit

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Charge Detection

The MT6305 charger block has a detection circuit that determinates if an adapter has been applied to the CHRIN pin and senses the CHRIN voltage. The maximum CHRIN voltage can be up to 15V but the detection circuit will report invalid_CHRIN when CHRIN>9V to protect the charging system. In other words, the charger block will do charging when CHRIN<=9V but stop charging when CHRIN>9V. However, applying 9V<CHRIN<15V won't damage the IC. Based on valid_CHRIN, if the adapter voltage exceeds the battery voltage by 3.0%, the CHRDET output will go high. If the adapter is then removed and the voltage at the CHRIN pin drops to only 3.0% above the VBAT pin, CHRDET goes low.

Pre-Charging mode

When the battery voltage is below the UVLO threshold, the charge current is in the pre-charging mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2V, a 10mA trickle current of MT6305 charges the battery internally. When the battery voltage exceeds 2V, the pre-charge current is enabled, which allows 10mV (typically) across the external current sense resistor. This pre-charge current can be calculated:

$$I_{PRE_CHARGING} = \frac{V_{SENSE}}{R1} = \frac{10mV}{R1} \qquad (2)$$

Constant Current Charging Mode

Once the battery voltage has exceeded the UVLO threshold the charger will switch to the constant current charging mode. The MT6305 allows 160mV (typically) across the external current sense resistor. This constant current can be calculated.

$$I_{CONSTANT} = \frac{V_{SENSE}}{R1} = \frac{160mV}{R1} \qquad (3)$$

If the battery voltage is below 4.2V of Li-ion battery charging (5.1V of NiMH battery charging), the battery will be in the constant current charging mode.

Constant Voltage Charging Mode

This mode is only applied to Li-ion battery charging. If the battery has reached the final charge voltage, a constant voltage is applied to the battery and keeps it at 4.2V. The charge termination is determined by the baseband chip internally, which will pull the CHRCNTL low to stop the charger.

Once the battery voltage exceeds 4.3V of Li-ion battery (5.1V of NiMH battery), a hardware over voltage protection (OV) should be activated and turn off the charger block of MT6305.

Pulsed Charging Algorithm

MT6305 is available to pulsed top-off charging algorithm by the CHRCNTL pin. The control signal is from baseband chipset to limit the charging duty cycle. This charging algorithm combines the efficiency of switch-mode chargers with the simplicity and low cost of linear chargers.

Battery Voltage Monitor

As the Table 2 shown, the relation of battery voltage and charger control with the responsible signals are listed. When Vbat <3.2V, an UVLO signal is active low. When Vbat >= 4.3, an OV signal is active and terminates charging. The disconnection of battery could be detected by BATDET pin. BATDET is pulled high internally when battery disconnected and terminates charging immediately.

Table 2. Charger and Voltage Detection

Vbat	CHRON	CHRCNTL	CHRDET	-UVLO	BATUSE	Charger Condition
Any Vbat	L	X	L	X	X	No-Charging
Vbat > 3.2V	X	L	X	H	X	No-Charging
Vbat < 3.2V	H	X	L	L	X	Pre-Charging
3.2V<Vbat<4.2V	H	H	H	H	L	CC mode
Vbat = 4.2V	H	H	H	H	L	CV mode
3.2V<Vbat	H	H	H	H	H	CC mode

Notes: OV terminates charging at 4.3V for Li-ion battery or 5.1V for NiMH battery.

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Applications Information

External Components Selection

Input Capacitor Selection

For each of input pins (VBAT) of MT6305, a local by-pass capacitor is recommended. Use a 10µF, low ESR capacitor. MLCC capacitors provide the best combination of low ESR and small size. Using a 10µF Tantalum capacitor with a small (1µF or 2.2µF) ceramic in parallel is an alternative low cost solution.

For charger input pin (CHRIN), a bypass 1µF ceramic capacitor is recommended.

LDO Capacitor Selection

The digital core, analog, memory LDOs require a 4.7µF capacitor, the digital IO, SIM TCXO LDOs require a 1µF capacitor and the, RTC LDO require a 0.22µF capacitor. Large value capacitor may be used for desired noise or PSRR issue. But take consideration of the settling time that is acceptable for system application. The MLCC X5R type capacitors must be used with VTCXO and VA LDOs for good system performance. For other LDOs, MLCC X5R type capacitors are also recommended to use.

RESET Capacitor Selection

RESET is held low at power-up until a delay time when LDOs are up. The delay is set by an external capacitor on RESCAP pin. It can be determinated by the Eq.(1).

A 100nF capacitor will produce a 200ms delay.

Setting the Charge Current

MT6305 is capable of charging battery. The charging current is programmed with an external sense resistor, Rsen. It is calculated as the Eq.(3). If the charge current is defined, Rsen can be found.

Appropriate sense resistors are available from the following vendors: Vishay Dale, IRC, Panasonic.

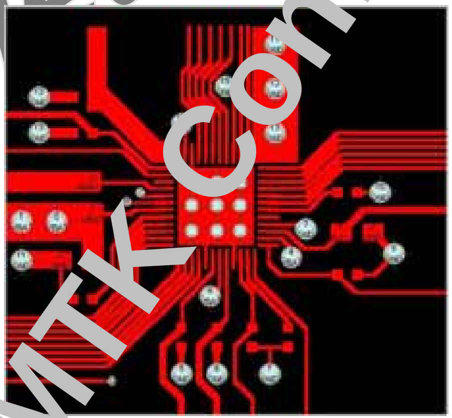

Figure 4. Top Layer of reference PCB Layout

Charger FET Selection

The PMOS FET selection of charger should considerate the minimum drain-source breakdown voltage (BVDS), the minimum turn-on threshold voltage (VGS), and current-handling and power-dissipation qualities.

These specifications can be calculated as below:

$V_{GS} = V_{CHRIN} - V_{GATEDRV}$

$V_{DS} = V_{CHRIN} - V_{DIODE} - V_{SENSE} - VBAT$

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR}}$$

$P_{DISS} = (V_{CHRIN}-V_{DIODE}-V_{SENSE}-VBAT) \times I_{CHR}$

Appropriate PMOS FETs are available from the following vendors: Siliconix, IR, Fairchild.

Charger Diode Selection

The diode shown in Figure 3 is used to prevent the battery from discharging through the PMOS's body diode into the charger's internal circuits. Choose a diode with a current rating high enough to handle the battery charging current and a voltage rating greater than Vbat.

Layout Guideline

Use the following general guild-line when designing printed circuit boards:

1. Split battery connection to the VBAT, AVBAT pins of MT6305. Locate the input capacitor as close to the pins as possible.
2. Va and Vtcxo capacitors should be returned to AGND.
3. Split the ground connection. Use separate traces or planes for the analog, digital, and power grounds (i.e. AGND, DGND, PGND pins of MT6305, respectively) and tie them together at a single point, preferably close to battery return.
4. Run a separate trace from the BATSNS pin to the battery to prevent voltage drop error in the measurement.
5. Kelvin-connect the charge current sense resistor by running separate traces to the BATSNS and ISENSE pins. Make sure that the traces are terminated as close to the resistor's body as possible.
6. Careful use of copper area, weight, and multi-layer constructibon will contribute to improve thermal performance.
7. See Fig4. for reference PCB layout. The thermal pad is attached to die substrate, so the thermal planes that the vias attach the package to **Must be connected to GND.**

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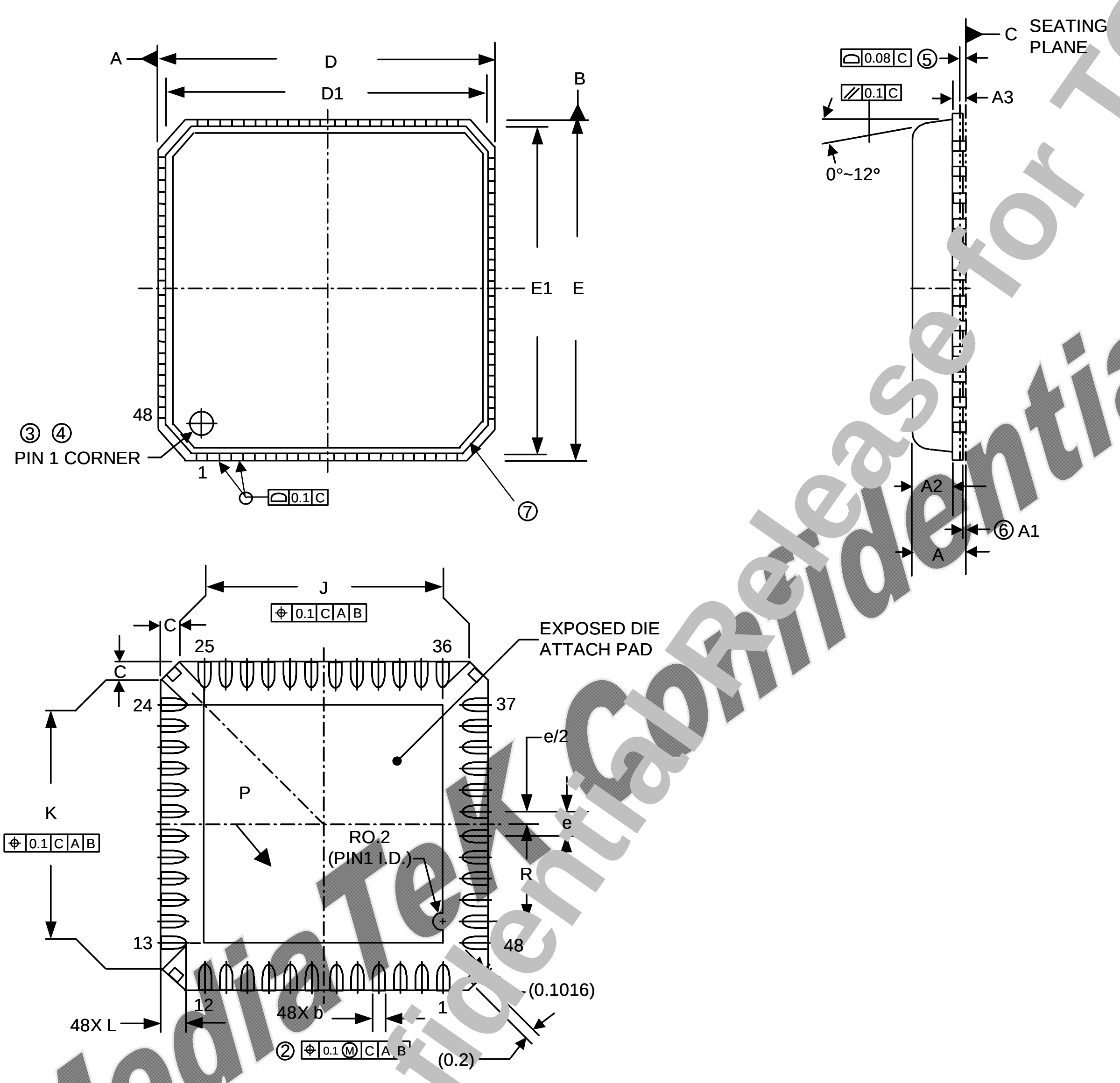
Package Information



Note:

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM)

② DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.

③ THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OF OTHER FEATURE OF PACKAGE BODY.

④ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

⑤ APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUED EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

⑥ APPLIED ONLY TO TERMINALS.

⑦ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

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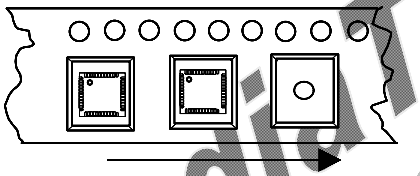
Package Information (continued)

Table 3. Package Dimension

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	-----	0.90	0.031	-----	0.035
A1	0	0.02	0.05	0	0.0008	0.002
A2	0.576	0.615	0.654	0.023	0.024	0.026
A3	0.203 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
C	0.24	0.42	0.60	0.009	0.017	0.024
D	7 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
E	7 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
e	0.5 BSC			0.020 BSC		
J	5.37	5.47	5.57	0.211	0.215	0.219
K	5.37	5.47	5.57	0.211	0.215	0.219
L	0.30	0.40	0.50	0.012	0.016	0.020
P	45° REF			45° REF		
R	2.185	2.285	2.385	0.086	0.090	0.094

Taping Specification



Feed Direction
Typical QFN Package Orientation

PACKAGE	Q'TY/REEL	Q'TY/TRAY
QFN-48	3,000 ea	260 ea

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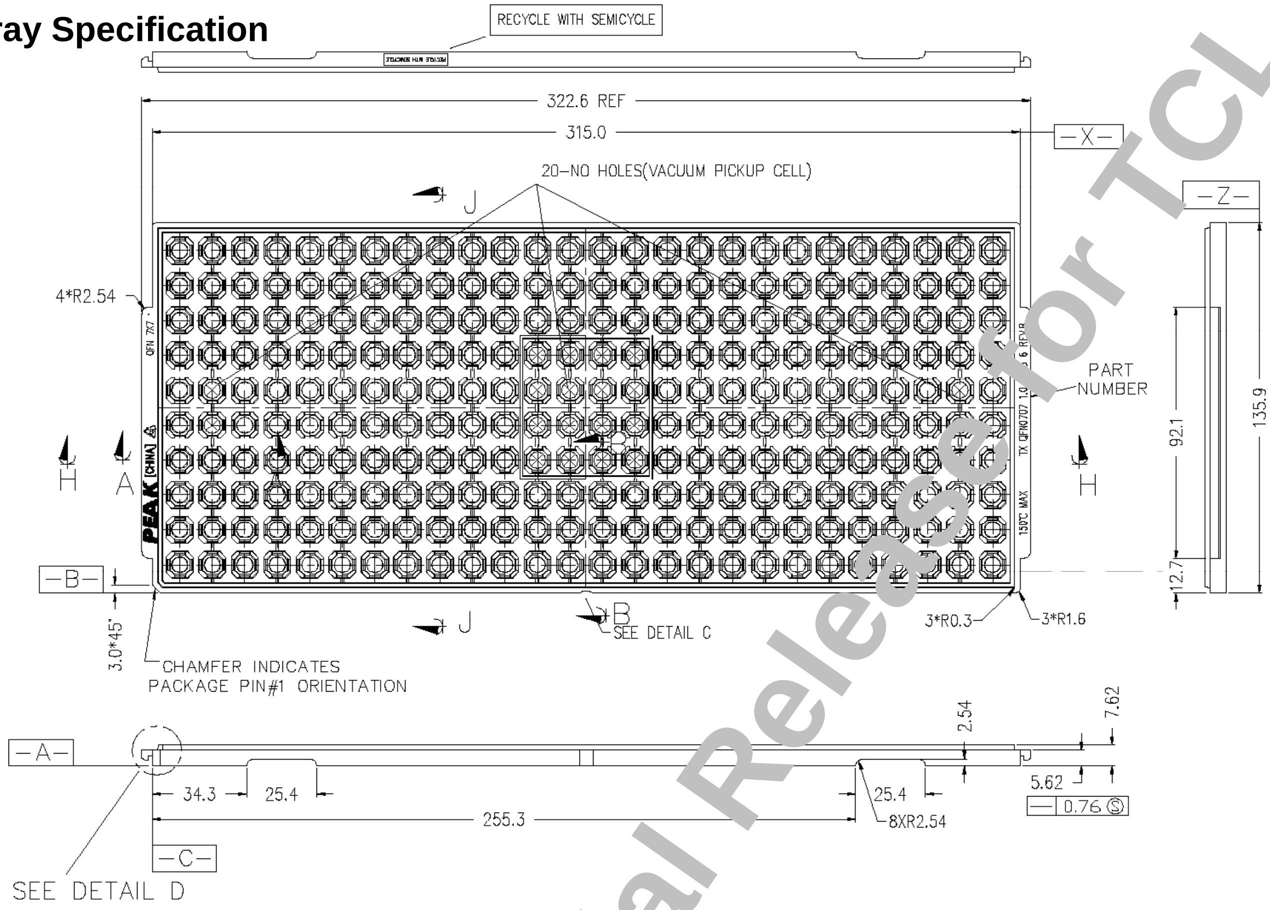
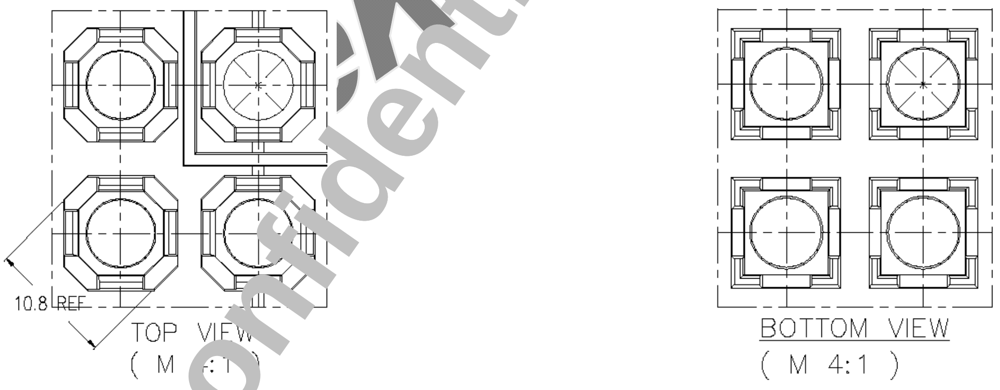
Tray Specification





NOTES :

1. MATERIAL - PP6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES - X.X=±0.25
   X.XX=±0.13
   DRAFT ANGLE FOR REFERENCE
   UNLESS OTHERWISE SPECIFIED.
4. ESD - SURFACE RESISTIVITY
   10^5 TO 10^{11} OHMS/SQ.
5. FOR PACKAGE - QFN 7X7
6. PART NO. : TX QFN0707 1.0 1026 6 REV.B
   (PLEASE INDICATE ON PURCHASE ORDER).

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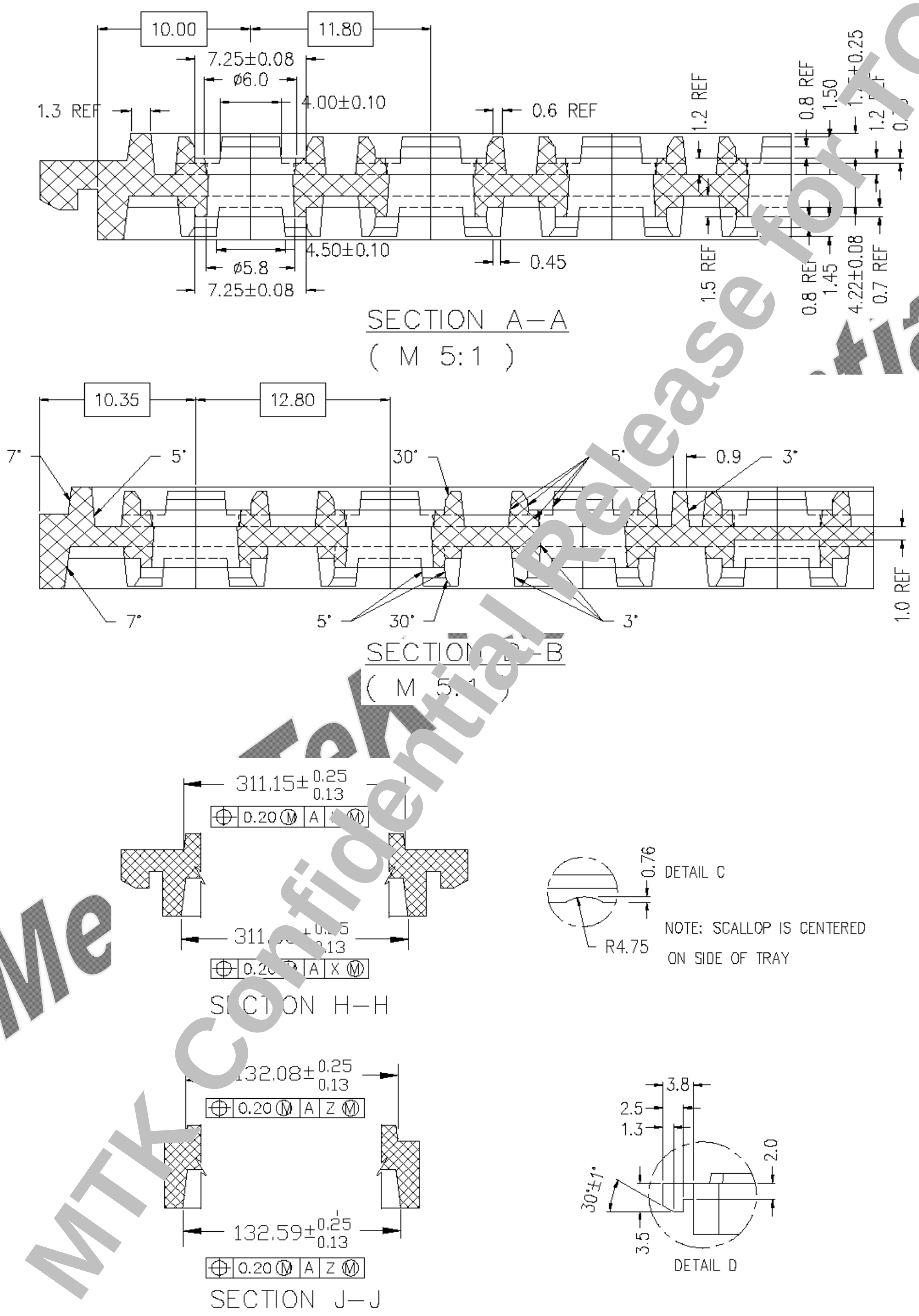
Tray Specification (continued)



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